Attorney Docket No.: SON-1718
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:

Yasukiyasu Sugano et al.

Confirmation No. 2204

Application No.: 09/478,812

Group Art Unit: 2815

Filed: January 7, 2000

Examiner: Eugene Lee

For: PROCESS FOR PRODUCING THIN FILM SEMICONDUCTORDEVICE AND LASER IRRADIATION APPARATUS

APPELLANT'S BRIEF

MS Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

This brief is an Appeal Brief under 37 C.F.R. §41.37 appealing the final decision of the Examiner dated August 28, 2006. Each of the topics required by 37 C.F.R. §41.37 is presented herewith and is labeled appropriately. A Notice of Appeal was filed on January 26, 2006 with a request for an extension of time for two months. This Appeal Brief is accompanied by a request for an extension of time for three months to file this appeal brief. Thus, this submission is timely.

This application relates to a process for producing a thin film semiconductor device and a laser irradiation apparatus. While this application has had a long and difficult prosecution, its divisional applications were favorably received. Thus, its first divisional application, Application No. 09/731,905 filed on December 8, 2000 was issued on October 14, 2003 as U.S. Pat. No. 6,632,711. Its second divisional application, Application No. 010/061,392, filed on February 4, 2002 was issued on February 17, 2004 as U.S. Pat. No. 6,693,258. Copies of those

two patents are appended to this Brief for the information of the Board when considering the issues in this Appeal.

It is believed that **no additional fees other than the extension fees are due**. M.P.E.P. §1208.03. However, if a fee is required, the Commissioner is hereby authorized to charge the fee to Deposit Account # 18-0013 and refer to SON-1718.

This brief is transmitted in triplicate.

This brief contains items under the following headings as required by 37 C.F.R. § 1.192 and M.P.E.P. § 1206:

I. REAL PARTY IN INTEREST

The real party in interest for this appeal is:

Sony Corporation of Tokyo, Japan ("Sony") is the real party in interest of the present application. An assignment of all rights in the present application to Sony was executed by the inventors and recorded by the U.S. Patent and Trademark Office at reel 010792, frame 0182.

II. RELATED APPEALS AND INTERFERENCES

There are no other pending and related appeals or interferences which will directly affect or be directly affected by or have a bearing on the Board's decision in this appeal of which the

Appellants are aware. A Decision on Appeal rendered on June 30, 2004 (copy included in the Related Appeals Appendix) affirmed the rejection of the examiner and resulted in an RCE filed on August 30, 2004.

III. STATUS OF CLAIMS

A. Total Number of Claims in Application

There are 14 claims pending in application, i.e. pending claims 11, 12, 17, 18, 27, 28, 39, 40, 53, 54, 63, 65, 73, and 74, of which each is an independent claim..

B. Current Status of Claims

The Application as filed contained claims 1 to 74. After canceling claims in view of a restriction requirement and other subsequent actions and amendments, only claims 11 to 12, 17 to 18, 27 to 28, 39 to 40, 53 to 54, 63, 65, and 73 to 74 are pending on appeal. No amendments have been made to the claims since the mailing of the Final Action of August 28, 2006 except for a deletion of a duplicative use of "wherein" in pending claim 11 to overcome an objection of the examiner; that change was made in the pending claims because of its non-controversial nature to satisfy an examiner requirement.

1. Claims canceled: 1-10, 13-16, 19-26, 29-38, 41-52, 55-62, 64 and 66-72
2. Claims withdrawn from consideration but not canceled: None
3. Claims pending: 11, 12, 17, 18, 27, 28, 39, 40, 53, 54, 63, 65, 73, 74
4. Claims allowed: None
5. Claims rejected: 11, 12, 17, 18, 27, 28, 39, 40, 53, 54, 63, 65, 73, 74

C. Claims On Appeal

The claims on appeal are claims 11, 12, 17, 18, 27, 28, 39, 40, 53, 54, 63, 65, 73, 74

IV. STATUS OF AMENDMENTS

Claims 11 to 12, 17 to 18, 27 to 28, 39 to 40, 53 to 54, 63 to 65, and 73 to 74 were initially examined after the above-mentioned RCE. A non-final Action dated February 15, 2006 was issued, and a response dated June 15, 2006 containing the claims here on appeal (except for a minor amendment to claim 11 to overcome an objection at final action) was submitted.. Following the Final Action, the Applicant's did not file a Response to Final Office Action, and the Notice of Appeal was thereafter filed.

Thus, the claims as presented in the Appendix represent all amendments that were made up until issuance of the Final Action.

V. SUMMARY OF INVENTION

Each of the pending independent claims is clear in defining the pending invention for each claim. For background, it can be noted that a first aspect of the present invention includes a thin film semiconductor device. The device includes a semiconductor thin film (e.g. layer 5, Fig. 7D), with a gate insulating film (combined film layers 2 and 3) accumulated on one surface thereof (lower surface of layer 5). A gate electrode (1) is accumulated on the semiconductor thin film (5) via the gate insulating thin film (2 and 3). The semiconductor thin film is formed by forming a 30 to 80 nm layer of amorphous silicon or polycrystalline silicon (layer 4 in Fig. 7B, page 39, lines 13 to 15). An energy beam is applied to a prescribed region, and a cross sectional shape of the energy beam is adjusted with respect to the prescribed region to irradiate the prescribed region in a single shot (page 10, lines 14 to 19; page 39, line 23 to page 40, line 6).

As shown in Fig. 11, plural units may be formed on the substrate (0). In this case, the irradiation step is conducted so that the substrate (0) is irradiated intermittently in order to convert the amorphous or polycrystalline material (4) to a polycrystalline material (page 45, lines 6 to 19). Further, a cross sectional shape of the energy beam is adjusted with respect to each unit to irradiate one or two or more units at a time by a single shot irradiation (page 45, last line to page 46, line 3).

At the time of formation, the amorphous silicon or polycrystalline silicon (4) has a first particle diameter; and after being irradiated with the energy beam, the semiconductor thin film

(4) is converted to polycrystalline silicon (5) having a larger particle diameter than the first particle diameter (page 48, lines 10 to 16).

Regarding the laser irradiation step, such step may be performed by irradiating the prescribed region of the substrate one or more times with a pulse of laser light having a constant cross sectional area and an emission time width from upstand to downfall of 50 ns or more (Fig. 23A, page 69 lines 6 to 11). Further, a desired change to the energy intensity of the laser light from upstand to downfall of the pulse is applied to said polycrystalline silicon (page 67, line 16 to page 68, last line).

According to the first embodiment of the invention, a thin film transistor (112, Fig. 8) is integrated and formed in a prescribed region by using the semiconductor thin film (5) thus converted to polycrystalline silicon as an active layer (page 43, lines 13 to 17). Due to the energy beam irradiation, characteristics of the thin film transistor are made uniform.

A second aspect of the invention involves a display device (Fig. 8, page 42, lines 12 to 15). The device includes a pair of substrates (101, 102) adhered to each other with a prescribed gap, and an electrooptical substance (103) maintained in the gap (page 42, lines 15 to 18). One of the substrates (102) includes a counter electrode, the other substrate (101) includes a pixel electrode (111) and a thin film transistor (112) driving the pixel electrode (111). The thin film transistor (112) includes a semiconductor thin film and a gate electrode accumulated on one surface of the semiconductor thin film through a gate insulating film as described above regarding the first aspect of the invention. The formation steps regarding the semiconductor thin film and the active region are also the same as described above.

A third aspect of the invention involves a thin film transistor having a laminated structure (Fig. 7, page 38, lines 17 to 19). The transistor includes a semiconductor thin film, a gate insulating film accumulated on one surface thereof, and a gate electrode accumulated on said semiconductor thin film through said gate insulating thin film, according to the same construction as defined above regarding the first aspect of the invention. Further, the formation steps described above are the same, although in this embodiment, the semiconductor thin film is accumulated by alternately repeating the film forming step and the irradiation step, without exposing the substrate to the air (Fig. 14, page 52, lines 9 to 12).

A fourth aspect of the invention involves a display device as described above regarding the second aspect of the invention, using the method described above regarding the third aspect

of the invention. According to the principle of accumulation of the semiconductor thin film, a semiconductor thin film (2A in Fig. 19A to F) is formed by forming a layer of about 20 nm amorphous silicon or polycrystalline silicon having a first particle diameter on a substrate (page 59, lines 5 to 8). The film (2A) is irradiating according to a prescribed region of the substrate (1A) with laser light having a prescribed cross sectional shape to convert to polycrystalline silicon having a larger particle diameter than the first diameter as described above. Then, additional semiconductor thin films are accumulated by alternately repeating the film forming step, where each additional formed film is about 1 nm (page 60, lines 19 to page 61, line 4).

As stated above, with regard to any of the aspects of the invention, it is preferred that during the irradiation steps, the substrate is maintained in a non-oxidative atmosphere (page 27, lines 12 to 13). Further, in one embodiment it is preferred that the irradiation step is performed under conditions where the substrate is uniformly heated (page 26, lines 16 to 20). In another embodiment, the substrate is cooled to a temperature lower than room temperature during the irradiation step (page 26, line 24 to page 27, line 4).

The foregoing detailed discussion of the features of the invention can be distilled at this point to prepare for a discussion of the dispositive issues raised in the final Action. Specifically, the examiner in his final Action considered the following limitations in the claims as product by process limitations (see the Final Action, page 3, top, page 4, first full paragraph regarding claim 28, and supporting discussion at pages 6 and 7 of the Final Action.):

1. The limitation "wherein said semiconductor thin film is accumulated without exposing said substrate to the air" as stated in a terminal portion of each of the dependent claims;

2. The limitation "irradiated with pulse laser light having an emission time width from upstand to downfall of at least 50 ns"; and

3. The limitation "substrate is cooled to a temperature lower than room temperature".

VI. ISSUES

The issues presented for consideration in this appeal are as follows:

(1) Whether the Examiner erred in rejecting each of the pending claims 11, 23. 27. 18. 27, 28, 39, 40, 53, 54, 63, 65, 73, and 74 by failing to give ANY weight to the "accumulated without exposing the substrate to air" limitation under 35 U.S.C. §102(b) or §103 as stated in any of sections 3, 5, 6 and 7 of the Final Action.?

(2) Whether the Examiner erred in rejecting claim 39 under either sections 35 U.S.C. §102 or §103(a) as allegedly being unpatentable by failing to give ANY weight to the "pulse laser light" limitation?

(3) Whether the Examiner erred in rejecting claim 73 under either sections §102 or §103(a) by failing to give any weight to the "substrate is cooled limitation".

Each of these issues will be discussed in turn. Because of the framing of the issues in terms of the examiner's ignoring limitations specifically stated in the claims, and thus ignoring structural implications of the stated limitations, it is less important in this appeal to argue specifically the merits of each rejection if such limitations were fully considered since no such rejection was made. Furthermore, by holding for the Appellant as to the first issue, the case is disposed of until a rejection is rephrased to include the ignored limitation of the first issue. As to the second and third issues, only certain claims are disposed of until a rejection is rephrased to include the ignored limitations or either of them.

VII. GROUPING OF CLAIMS

For purposes of this appeal brief only, and without conceding the teachings of any prior art reference, the claims are not grouped, but rather each of the inventions of each independent claims stands or falls separately in that at least one of its limitations has not been considered by the examiner.. The reasoning for the grouping of the claims is evident in light of the following arguments.

VIII. ARGUMENTS

Introduction

For at least the following reasons, Appellant submits that these rejections are both technically and legally unsound and should therefore be reversed.

The claims that are pending for the Examiner's consideration in this application are apparatus claims that are directed to the thin film semiconductor devices that result from an

inventive method. It is recognized that process limitations in product claims are not given any patentable weight **unless** they ascribe a structural feature to the resulting semiconductor chip. Therefore, the following discussion establishes how the process steps in the present claims do in fact ascribe a structural feature to the semiconductors made thereby, which distinguish the semiconductors from those of the prior art.

While the following discussion emphasizes features of the claims that were ignored by the examiner as product by process limitations, it should be noted that each claim is a combination of features, including the features at issue, so that the structure of each claim can be considered in its entirety.

B. All Pending Claims Are Prima Facie Patentable Over the Applied Art When The Limitation "Accumulation Without Exposing the Film to Air" is Considered.

MPEP §2113 clearly suggests that the structure implied by process limitations should be considered when assessing the patentability of claims. Here, the terminal limitation of each of the pending claims on appeal refers to a film that is accumulated without exposing the substrate to air. Thus, a non-oxidized structure in the accumulated film thickness is implied and not shown in the art. See In re Garnero, 412 F. 2d 276, 279; 162 USPQ 221, 223 (CCPA 1979) discussed in MPEP §2113. Here, each of the inventions defined by each of the independent claims defines a structure having a particular characteristic, i.e. one that is implied by accumulation without exposing the substrate to air.

The only argument advanced by the examiner is that "such a process, as stated in the applicant's claims, does not structurally differentiate the thin film of Noguchi from the thin film in the Applicant's claims". This finding is respectfully traversed in that nothing in Noguchi suggests that his thin film is accumulated without exposing the substrate to air, as limited in each of the pending claims, see page 6 of the Final Action. In contrast, according to the specification at pages 51 et seq. and Fig. 14, the film forming step and the laser annealing step are alternately repeated to accumulate the semiconductor thin films without exposing the substrate to the air.

Why? By employing such a repeating process in vacuum (or inert gas) a step of removing contamination substances and dusts from the air can be eliminated and thus improvement in throughput is considerable. Crystals of high quality can be formed. See pages

52 and 53 of the specification as filed. See also Fig. 15 and pages 53 and 54. There are other examples throughout the specification showing the importance of the accumulation feature, all supporting the feature that the implied structure is different from one that is processed differently.

Each of independent claims recites that a thin film semiconductor is formed by irradiating an amorphous semiconductor substrate with an energy beam that has an adjusted cross sectional shape so that a region of the substrate is irradiated with a single shot, so that a resultant polycrystalline silicon substrate is uniform in its crystallinity. Throughout the present specification (i.e., page 51, lines 7 to 12) it is repeatedly taught that by irradiating the entirety of the unit size of the thin film semiconductor device that the crystallization of the silicon film is made continuous, avoiding the formation of borders in the crystallized silicon. The specification also teaches that such borders are the product of conventional crystallization processes that involve the piecemeal irradiation of several adjacent regions of the unit size of the semiconductor device. The borders in the conventional process are the result of slight overlapping of regions that are separately irradiated. Consequently, the single shot irradiation process of the present invention does ascribe a structural limitation to the resultant thin film semiconductor that sets the structure apart from thin film semiconductors that are formed by irradiation of several adjacent regions in a unit area.

Failure to give weight to the "accumulated without exposure to air limitation" is inconsistent with the principles of sections 102 and 103 of the Patent Act because the ignored limitation is neither expressly or inherently described in a single prior art reference. "A claim is anticipated [under 35 U.S.C. § 102] only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." Verdegaal Bros. v. Union Oil Co. of California, 2 U.S.P.Q.2d 1051, 1053 (Fed. Cir. 1987) (emphasis added). See M.P.E.P. § 2131. Likewise, "[t]o establish prima facie obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. In re Royka, 490 F.2d 981, 180 USPQ 580 (CCPA 1974)." M.P.E.P. § 2143.03. Accord. M.P.E.P. § 706.02(j). Because the above-discussed features of the claims are neither taught nor suggested by the prior art of record, it is respectfully submitted that the rejections of the claims cannot be sustained for failure to consider the accumulation without air exposure feature.

Accordingly, all claims are to be considered with the subject limitation in place, and are urged to be patentable over the art applied. At this juncture, a reversal of the position of the examiner by this Board will result in a remand for consideration of the patentability of the claims over art then cited to include this missing feature.

C. Failure to Consider the "Irradiated with Pulse Light" Limitation is Error

The second full paragraph at the top of page 3 of the Final Action states, as to claim 39, that the limitation "irradiated with pulse laser light having an emission time width from upstand to downfall of at lest 50 ns" is a product by process limitation. According to the specification and the foregoing explanation, the limitation on what is the polycrystalline silicon as explained is a structural limitation and is understood in the art to be a structural limitation. The specification as filed is replete with discussions of converting amorphous silicon to polycrystalline silicon according to this radiation technique; the fact that the irradiation occurs with pulse laser light having the stated emission time width from upstand to downfall as stated in the first wherein clause of claim 39 imparts a patentable feature to the claim. For example, the discussion of Fig. 18 at pages 57 to 58 and Figs. 21A to Fig 23 at pages 65 to 69 of the specification as filed point out structural changes that result from the stated pulse characteristics. See also pages 92 and 93 of the specification as filed. Accordingly, as in the test of MPEP §2113, the structure implied by that stated limitation should be considered. See In re Garnero, supra.

D. The Failure to Consider the "Cooling" Limitation in Claim 73 is Error.

The applicable test of MPEP §2113 and In re Garnero, supra are also applicable here. The examiner argued that the limitation "substrate is cooled to a temperature lower than room temperature" is a product by process limitation. As before, however, that limitation implies a structure for the substrate that must be considered in assessing the patentability of claim 73. That structure is discussed at pages 94 et seq. of the specification as filed in terms of the conversion of the semiconductor film contained in the irradiated region to a polycrystalline material. This feature increases the probability of generation of crystal nuclei so that the number

of the crystal particles contained in the semiconductor thin film having uniform crystal particle diameters can be obtained so that the thin film can be used as an active layer.

IX. CONCLUSION

In view of the foregoing reasons, Appellant submits that the final rejection of claims 11 to 12, 17 to 18, 27 to 28, 39 to 40, 53 to 54, 63, 65, and 73 to 74 is improper and should not be sustained. Therefore, a reversal of the Final Rejection of August 28, 2004, as to claims 11 to 12, 17 to 18, 27 to 28, 39 to 40, 53 to 54, 63, 65, and 73 to 74, is respectfully requested.

Dated: June 26, 2007

Respectfully submitted,

By_____
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APPENDIX A

A complete listing of all pending claims is presented.

1. (Cancelled)

2. (Cancelled)

3. (Cancelled)

4. (Cancelled)

5. (Cancelled)

6. (Cancelled)

7. (Cancelled)

8. (Cancelled)

9. (Cancelled)

10. (Cancelled)

11. (Currently Amended) A thin film semiconductor device comprising a semiconductor thin film, a gate insulating film accumulated on one surface thereof, and a gate electrode accumulated entirely within a prescribed region of said semiconductor thin film through said gate insulating thin film,

wherein said semiconductor thin film includes polycrystalline silicon having a first particle diameter, wherein said polycrystalline silicon is an irradiation converted substrate that in the prescribed region has a 30 to 80 nm layer of amorphous silicon or polycrystalline silicon having a second particle diameter that is larger than said first particle diameter;

a thin film transistor integrated in said prescribed region through said semiconductor thin film, wherein said converted polycrystalline silicon semiconductor film has a single-shot irradiated region, and

a cross sectional shape of said energy beam is adjusted with respect to said prescribed region to consist of irradiating said prescribed region in its entirety at a time by a single shot irradiation, so that characteristics of said thin film transistor are made uniform; and

whereby said single-shot irradiated region is a borderless irradiated region; and

[wherein] wherein said semiconductor thin film is accumulated without exposing said substrate to air to accumulate said semiconductor thin film.

12. (Previously Presented) A display device comprising a pair of substrates adhered to each other with a prescribed gap, and an electrooptical substance maintained in said gap, one of said substrates comprises a counter electrode, the other substrate comprises a pixel electrode and a thin film transistor driving said pixel electrode, and said thin film transistor comprises a semiconductor thin film and a gate electrode accumulated entirely within a prescribed region of one surface of said semiconductor thin film through a gate insulating film,

wherein said semiconductor thin film includes polycrystalline silicon having a first particle diameter, wherein said polycrystalline silicon is an irradiation converted substrate that in the prescribed region has a 30 to 80 nm layer of amorphous silicon or polycrystalline silicon having a second particle diameter that is larger than said first particle diameter;

a thin film transistor integrated in said prescribed region through said semiconductor thin film wherein said converted polycrystalline silicon semiconductor film has a single-shot irradiated region; and

a cross sectional shape of said energy beam is adjusted with respect to said prescribed region to consist of irradiating said prescribed region in its entirety at a time by a single shot irradiation, so that characteristics of said thin film transistor are made uniform; and

whereby said single-shot irradiated region is a borderless irradiated region; and

wherein said semiconductor thin film is accumulated without exposing said substrate to air to accumulate said semiconductor thin film.

13. (Cancelled)

14. (Cancelled)

15. (Cancelled)

16. (Cancelled)

17. (Previously Presented) A thin film semiconductor device comprising a semiconductor thin film, a gate insulating film accumulated on one surface thereof, and a gate electrode accumulated entirely within a unit of said semiconductor thin film through said gate insulating thin film,

wherein said semiconductor thin film includes polycrystalline silicon having a first particle diameter, wherein said polycrystalline silicon is an irradiation converted substrate having a 30 to 80 nm layer of amorphous silicon or polycrystalline silicon having a second particle diameter that is larger than said first particle diameter,

wherein at least one unit of the semiconductor thin film is a single-shot irradiated unit based on a cross sectional shape of said energy beam, and

a thin film transistor is integrated and formed in said at least one unit thus subjected to irradiation at a time; and

whereby said irradiated region is a borderless irradiated region; and

whereby said film is accumulated without exposing said substrate to air, to accumulate said semiconductor thin film

18. (Previously Presented) A display device comprising a pair of substrates adhered to each other with a prescribed gap, and an electrooptical substance maintained in said gap, one of said substrate comprises a counter electrode, the other substrate comprises a pixel electrode and a thin film transistor driving said pixel electrode, and said thin film transistor comprises a semiconductor thin film and a gate electrode accumulated entirely within a unit of one surface of said semiconductor thin film through a gate insulating film,

wherein said semiconductor thin film includes polycrystalline silicon having a first particle diameter, wherein said polycrystalline silicon is an irradiation converted 30 to 80 nm layer of amorphous silicon or polycrystalline silicon having a second particle diameter that is larger than said first particle diameter,

wherein at least one unit of the semiconductor thin film is a single-shot irradiated unit, based on a cross sectional shape of said energy beam, and

a thin film transistor is integrated and formed in said at least one unit thus subjected to irradiation at a time; and

whereby said irradiated region is a borderless irradiated region; and

wherein said film is accumulated without exposing said substrate to air, to accumulate said semiconductor thin film.

19. (Cancelled)

20. (Cancelled)

21. (Cancelled)

22. (Cancelled)

23. (Cancelled)

24. (Cancelled)

25. (Cancelled)

26. (Cancelled)

27. (Previously Presented) A thin film transistor having a laminated structure comprising a semiconductor thin film, a gate insulating film accumulated on one surface thereof, and a gate electrode accumulated entirely within a prescribed region of said semiconductor thin film through said gate insulating thin film,

wherein said semiconductor thin film includes polycrystalline silicon having a first particle diameter, wherein in the prescribed region said polycrystalline silicon has an irradiation converted 30 to 80 nm layer of amorphous silicon or polycrystalline silicon having a second particle diameter that is larger than said first particle diameter, and

said semiconductor thin film is accumulated without exposing said substrate to the air; and

whereby said irradiated region is a borderless irradiated region.

28. (Previously Presented) A display device comprising a pair of substrates adhered to each other with a prescribed gap, and an electrooptical substance maintained in said gap, one of said substrate comprises a counter electrode, the other substrate comprises a pixel electrode and a thin film transistor driving said pixel electrode, and said thin film transistor comprises a semiconductor thin film and a gate electrode accumulated entirely within a prescribed region of one surface of said semiconductor thin film through a gate insulating film,

wherein said semiconductor thin film includes polycrystalline silicon having a first particle diameter, wherein said polycrystalline silicon is an irradiation converted substrate that in the prescribed region has a 30 to 80 nm layer of amorphous silicon or polycrystalline silicon having a second particle diameter that is larger than said first particle diameter; and

said semiconductor thin film is accumulated by alternately repeating said film forming step, where each additional formed film is about 1 nm, and said irradiation step without exposing said substrate to the air; and

whereby said irradiated region is a borderless irradiated region.

29. (Cancelled)

30. (Cancelled)

31. (Cancelled)

32. (Cancelled)

33. (Cancelled)

34. (Cancelled)

35. (Cancelled)

36. (Cancelled)

37. (Cancelled)

38. (Cancelled)

39. (Previously presented) A thin film transistor having a laminated structure comprising a semiconductor thin film, a gate insulating film accumulated on one surface thereof, and a gate electrode accumulated entirely within a prescribed region of said semiconductor thin film through said gate insulating film,

wherein said semiconductor thin film includes polycrystalline silicon, wherein said polycrystalline silicon is an irradiation converted substrate having a 30 to 80 nm layer of non-single crystal silicon, said converted polycrystalline silicon corresponds to a cross-sectional area of the substrate irradiated with pulse laser light having an emission time width from upstand to downfall of at least 50ns, and

a desired change to said energy intensity of said laser light from upstand to downfall of said pulse is applied to said polycrystalline silicon; and

whereby said irradiated region is a borderless irradiated region; and

wherein [said film forming step and said irradiating step are alternately repeated without exposing said substrate to air, to accumulate] said semiconductor thin film is accumulated without exposing said substrate to air.

40. (Previously Presented) A display device comprising a pair of substrates adhered to each other with a prescribed gap, and an electrooptical substance maintained in said gap, one of said substrate comprises a counter electrode, the other substrate comprises a pixel electrode and a thin film transistor driving said pixel electrode, and said thin film transistor comprises a semiconductor thin film and a gate electrode accumulated entirely within a prescribed region of one surface of said semiconductor thin film through a gate insulating film,

wherein said semiconductor thin film includes polycrystalline silicon, wherein said polycrystalline silicon is an irradiation converted substrate having a 30 to 80 nm layer of non-single crystal silicon, said converted polycrystalline silicon corresponds to a cross-sectional area of the substrate irradiated with pulse laser light having an emission time width from upstand to downfall of at least 50ns,

a desired change to said energy intensity of said laser light from upstand to downfall of said pulse is applied to said polycrystalline silicon; and

whereby said irradiated region is a borderless irradiated region; and

wherein said film without exposing said substrate to air, to accumulate said semiconductor thin film.

41. (Cancelled)

42. (Cancelled)

43. (Cancelled)

44. (Cancelled)

45. (Cancelled)

46. (Cancelled)

47. (Cancelled)

48. (Cancelled)

49. (Cancelled)

50. (Cancelled)

51. (Cancelled)

52. (Cancelled)

53. (Previously Presented) A thin film transistor having a laminated structure comprising a semiconductor thin film, a gate insulating film accumulated on one surface thereof, and a gate electrode accumulated entirely within a prescribed region of said semiconductor thin film through said gate insulating film,

wherein said semiconductor thin film includes polycrystalline silicon, wherein said polycrystalline silicon is an irradiation converted substrate having a 30 to 80 nm layer of non-single crystal silicon, said converted polycrystalline silicon corresponds to a cross-sectional area of the substrate in the prescribed region that is irradiated with pulse laser light having an emission time width of at least 50ns in a non-oxidative atmosphere,

whereby said irradiated region is a borderless irradiated region; and

wherein [said film forming step and said irradiating step are alternately repeated without exposing said substrate to air, to accumulate] said semiconductor thin film is accumulated without exposing said substrate to air.

54. (Currently amended) A display device comprising a pair of substrates adhered to each other with a prescribed gap, and an electrooptical substance maintained in said gap, one of said substrate comprises a counter electrode, the other substrate comprises a pixel electrode and a thin film transistor driving said pixel electrode, and said thin film transistor comprises a semiconductor thin film and a gate electrode accumulated entirely within a prescribed region of one surface of said semiconductor thin film through a gate insulating film,

wherein said semiconductor thin film includes polycrystalline silicon, wherein said polycrystalline silicon is an irradiation converted substrate having a 30 to 80 nm layer of non-single crystal silicon, said converted polycrystalline silicon corresponds to a cross-sectional area

of the substrate in the prescribed region that is irradiated with pulse laser light having an emission time width of at least 50ns,

whereby said irradiated region is a borderless irradiated region; and

wherein said film is accumulated without exposing said substrate to air, to accumulate said semiconductor thin film.

55. (Cancelled)

56. (Cancelled)

57. (Cancelled)

58. (Cancelled)

59. (Cancelled)

60. (Cancelled)

61. (Cancelled)

62. (Cancelled)

63. (Previously Presented) A thin film transistor having a laminated structure comprising a semiconductor thin film, a gate insulating film accumulated on one surface thereof, and a gate electrode accumulated entirely within a prescribed region of said semiconductor thin film through said gate insulating film,

wherein said semiconductor thin film includes polycrystalline silicon, wherein said polycrystalline silicon is an irradiation converted substrate having a 30 to 80 nm layer of non-single crystal silicon, said converted polycrystalline silicon corresponds to a cross-sectional area of the substrate in the prescribed region that is irradiated with pulse laser light having an emission time width of at least 50ns when said substrate is uniformly heated;

whereby said irradiated region is a borderless irradiated region; and

wherein said semiconductor thin film is accumulated without exposing said substrate to air.

64. (Cancelled)

65. (Previously Presented) A display device comprising a pair of substrate adhered to each other with a prescribed gap, and an electrooptical substance maintained in said gap, one of said substrate comprises a counter electrode, the other substrate comprises a pixel electrode and a thin film transistor comprises a semiconductor thin film and a gate electrode accumulated entirely within a prescribed region of one surface of said semiconductor thin film through a gate insulating film,

wherein said semiconductor thin film includes polycrystalline silicon, wherein said polycrystalline silicon is an irradiation converted substrate having a 30 to 80 nm layer of non-single crystal silicon, said converted polycrystalline silicon corresponds to a cross-sectional area of the substrate in the prescribed region that is irradiated with pulse laser light having an emission time width of at least 50ns when said substrate is uniformly heated,

whereby said irradiated region is a borderless irradiated region; and

wherein said semiconductor thin film is accumulated without exposing said substrate to air.

66. (Cancelled)

67. (Cancelled)

68. (Cancelled)

69. (Cancelled)

70. (Cancelled)

71. (Cancelled)

72. (Cancelled)

73. (Previously Presented) A thin film transistor having a laminated structure comprising a semiconductor thin film, a gate insulating film accumulated on one surface thereof, and a gate electrode accumulated entirely within a prescribed region of said semiconductor thin film through said gate insulating film,

wherein said semiconductor thin film includes polycrystalline silicon, wherein said polycrystalline silicon is an irradiation converted substrate having a 30 to 80 nm layer of non-

single crystal silicon, said converted polycrystalline silicon corresponds to a cross-sectional area of the substrate in the prescribed region that is irradiated with pulse laser light having an emission time width of at least 50ns when said substrate is cooled to a temperature lower than room temperature,

whereby said irradiated region is a borderless irradiated region; and

wherein said film is accumulated without exposing said substrate to air, to accumulate said semiconductor thin film.

74. (Previously Presented) A display device comprising a pair of substrates adhered to each other with a prescribed gap, and an electrooptical substance maintained in said gap, one of said substrates comprises a counter electrode, the other substrate comprises a pixel electrode and a thin film transistor driving said pixel electrode, and said thin film transistor comprises a semiconductor thin film and a gate electrode accumulated entirely within a prescribed region of one surface of said semiconductor thin film through a gate insulating film,

wherein said semiconductor thin film includes polycrystalline silicon, wherein said polycrystalline silicon is an irradiation converted substrate having a 30 to 80 nm layer of non-single crystal silicon, said converted polycrystalline silicon corresponds to a cross-sectional area of the substrate in the prescribed region that is irradiated with pulse laser light having an emission time width from upstand to downfall of at least 50ns when said substrate is cooled to a temperature lower than room temperature,

whereby said irradiated region is a borderless irradiated region; and

wherein said film is accumulated without exposing said substrate to air, to accumulate said semiconductor thin film.

APPENDIX B EVIDENCE APPENDIX

There is no other evidence, other than the MPEP citation and In re Garnero copies attached which will directly affect of have a bearing on the Board's Decision in this appeal.

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We agree with the board's conclusion. It is clear from the above quotations that none of the so-called corroborating witness affidavits makes any reference to even one of the process limitations of the count. As the appellee said to the board, "The probative significance of these averments is nil * * *." Nothing is left except the averments of the inventor himself and his own notebook. Examination of the notebook shows that it was kept by Kistler himself and is unwitnessed. The supporting witnesses said no more, in effect, than that they had seen the notebook in his laboratories, along with the equipment and bottles. They did not say they knew anything of its contents. Therefore, they have not corroborated anything it contains.

Consideration of Kistler's Supplemental Brief shows that his theory of this case is that he does not have to *prove* his facts at this stage of the interference but only give rise to an *inference* or show a *possibility* that he could prove them later, which he says should suffice to prevent summary judgment:

> * * * Appellant should be entitled to a trial on the merits. For now, it is sufficient that we can say when considering the purpose for which the affidavits were made, that there is a reasonable *possibility* that the corroborating affiants *possessed* the knowledge required. [Emphasis ours.]
>
> * * *

Moreover, a determination of whether or not the corroborating affiants had acutal knowledge of the steps of the process or of testing is premature; such a determination bears only upon the weight to be given their subsequent testimony.

We cannot accept this procedural theory. To do so would entirely vitiate the purposes of Rules 204(c) and 228 and allow mere uncorroborated assertions to take the place of proof of acts and circumstances adequate to overcome Weber's March 9, 1960, filing date.

The decision of the board is *affirmed*.

Court of Customs and Patent Appeals

In re GARNERO

No. 8172 Decided June 26, 1969

PATENTS

1. Claims—Article defined by process of manufacture (§ 20.15)

Mere presence of method limitation in article claim which is otherwise allowable does not so poison claim as to render it unpatentable.—In re Garnero (CCPA) 162 USPQ 221.

2. Claims—"Comprising," "Consisting," etc. (§ 20.30)

"Consisting essentially of" terminology in claim excludes additional unspecified ingredients which would affect basic and novel characteristics of product defined in balance of claim.—In re Garnero (CCPA) 162 USPQ 221.

Particular patents—Structural Material

Garnero, Structural Material of Expanded Minerals and Method for Manufacture, claims 1 and 9 of application allowed.—In re Garnero (CCPA) 162 USPQ 221.

Appeal from Board of Appeals of the Patent Office.

Application for patent of Anthony L. Garnero, Serial No. 381,145, filed July 8, 1964; Patent Office Group 160. From decision rejecting claims 1 and 9, applicant appeals. Reversed.

See also 145 USPQ 457.

HERMAN HERSH and MCDOUGALL, HERSH, SCOTT & LADD, both of Chicago, Ill. (GEORGE A. DEGNAN, Washington, D. C., of counsel) for appellant.

JOSEPH SCHIMMEL (FRED W. SHERLING of counsel) for Commissioner of Patents.

Before RICH, Acting Chief Judge, HOLTZOFF and MCLAUGHLIN, Judges, sitting by designation, and ALMOND and BALDWIN, Associate Judges.

BALDWIN, Judge.

This appeal is from the Patent Office Board of Appeals decision affirming the examiner's rejection of two claims[1] of appellant's application[2] as unpatentable

[1] The rejections of only claims 1 and 9 are pursued on appeal here.

[2] Serial No. 381,145, filed July 8, 1964, for "Structural Material of Expanded Minerals and Method for Manufacture," allegedly a continuation of application serial No. 714,831, filed February 12, 1958, for "Structural Material of Expanded Minerals and Method for Manufacturing." The parent application was before this

under 35 U.S.C. 103, claim 1 being rejected on Thomas [3] in view of Pierce [4] and claim 9 being rejected on the same combination of references further in view of Ford.[5] No claim has been allowed.

The Invention

The invention relates to a thermal insulation panel formed from expanded perlite particles. The particles are held together without any additional material, such as an external bonding agent, by interfusion between the surfaces of the perlite particles. Interfusion is effected by taking the initially unexpanded perlite particles and heating them rapidly for expansion so that combined water associated with the particles is released as a vapor which operates as a flux which enables the particles to become stuck together at temperatures as low as 1400 °F.[6] The specification describes the product as "having a density which may vary from 1 pound per cubic foot to as much as 80 pounds per cubic foot while still maintaining a porosity and a mass integrity sufficient to enable use thereof as a structural insulation material."

Claims 1 and 9 read:

1. A composite, porous, thermal insulation panel characterized by dimensional stability and structural strength consisting essentially of expanded perlite particles which are interbonded one to another by interfusion between the surfaces of the perlite particles while in a pyroplastic state to form a porous perlite panel.

9. An insulation panel as claimed in Claim 1 in which the panel is formed in cross-section with layers of different densities.

The References

Thomas discloses a pipe insulating composition which utilizes sodium silicate as a binding agent to hold already expanded perlite particles together, with sodium chloride being used as a setting agent. A mixture of the expanded perlite, the sodium silicate binder, and the sodium chloride setting agent are subjected to a compression from 5 to 7 tons per square foot, at ambient temperature, to produce articles formed of the composition. Prior to compression, Thomas' aggregate mixture has a density of 4 to 10 pounds per cubic foot.

Pierce discloses a building material utilizing expanded perlite particles which are mixed with hot hydrated lime (CaO) at a temperature of about 300° F. Pierce states that "the exterior of the granules reacts chemically to bind the entire mass together." The specification discloses that the end product may have a density of 40-50 pounds per cubic foot.

Ford discloses cellular glass pellets having a core of highly cellulated glass, an intermediate layer of less highly cellulated glass, and an outer layer of substantially uncellulated glass, thus demonstrating a panel having a cross-section of varying density.

The Rejection

Sustaining the examiner's rejection of claim 1 as being unpatentable over Thomas in view of Pierce under 35 U.S.C. 103, the board stated:

> The language used by Pierce is considered to be readable on "interbonding by interfusion" as expressed in the claims at issue. Albeit that the condition limitations appear to differ somewhat from the details of the process described by the patentees, we are apprised of no facts which would lead us to conclude that the instantly claimed product necessarily would be patentably unique when compared to that resulting from the prior art methods.

The board rejected arguments by appellant that the inclusion in the claim of the phrase "consisting essentially of" would exclude the presence of an ex-

court in In re Garnero, 52 CCPA 1370, 345 F.2d 589, 145 USPQ 457 (1965), and we there affirmed the rejection of claims directed to a method of manufacturing an expanded perlite structure as being obvious under 35 U.S.C. 103 in view of certain, different prior art cited in that case.

[3] U. S. Patent 2,600,812, issued June 17, 1952.

[4] U. S. Patent 2,517,235, issued August 1, 1950.

[5] U. S. Patent 2,691,248, issued October 12, 1954.

[6] Thus, appellant's specification states:

> Fusion believed to be necessary for adhesion occurs with the average perlite at a temperature within the range of 2000-2200° F. It has been found, however, that the combined water which is released as a vapor when the perlite particles are heated to a pyroplastic state operates as a flux which enables the desired stickiness to develop for agglomeration when the particles are heated to a temperature as low as 1400° F. but preferably at a temperature above 1600° F. Thus agglomeration can be achieved at a temperature starting at 1400° F. Best adhesions and expansions are secured when the particles are heated to a temperature above 1800° F. Thus the preferred conditions for operation from the standpoint of expansion and agglomeration will reside in heating the particles to a temperature of 1800-2200° F.

ternal binder and thus distinguish from the composition of Thomas which uses a sodium silicate binder and that the phrase "expanded perlite particles which are interbonded one to another by interfusion between the surfaces" distinguishes from the chemical bonding of Pierce which employs lime as an additional ingredient. Instead the board noted the existence of other claims (now cancelled) adding other limitations to claim 1 and stated:

> [T]he recital of "consisting essentially" renders a claim open only for the inclusion of unspecified ingredients which would not materially affect the basic and novel characteristics of the product defined in the balance of the claim. * * * Where, as here, other claims indicate that particular components are not excluded by the words "consisting essentially of", appellant's arguments as to the existence of diverse reaction mechanisms in the prior art processes cannot be accepted as conclusive of a factual patentable distinction in his claimed product.

The examiner's rejection of claim 9 on the ground that the feature of different densities in different layers would be an obvious modification in view of Ford, was affirmed by the board in that:

> Appellant has urged no patentable merit in the specific modifications set forth in claims 5 through 9, and we perceive none.

Opinion

On appeal the solicitor's position appears to be that the only distinction between appellant's *product* and the *products* of the prior art is the *process* by which appellant's product is made; and, as that *process* has been found to be unpatentable in our previous decision of In re Garnero, 52 CCPA 1370, 345 F.2d 589, 145 USPQ 457 (1965), then the *product* claims are likewise unpatentable. The solicitor is in effect reading claim 1, which recites "expanded perlite particles which are interbonded one to another by interfusion between the surfaces of the perlite particles while in a pyroplastic state to form a porous perlite panel," as a product claim containing a process limitation and then applying the rationale expressed by this court in In re Stephens, 52 CCPA 1409, 345 F.2d 1020, 145 USPQ 656 (1965); and In re Dilnot, 49 CCPA 1015, 300 F.2d 945, 133 USPQ 289 (1962).

The trouble with the solicitor's approach is that it necessarily assumes that claim 1 should be construed as a product claim containing a process, rather than structural, limitation. However, it seems to us that the recitation of the particles as "interbonded one to another by interfusion between the surfaces of the perlite particles" is as capable of being construed as a structural limitation as "intermixed," "ground in place," "press fitted," "etched," and "welded," all of which at one time or another have been separately held capable of construction as structural, rather than process, limitations.[7] The correct inquiry therefore, it appears to us, is whether the product defined by claim 1 is patentably distinguishable over the disclosures of Thomas and Pierce in view of the *structural* limitation defining the panel as "consisting essentially of expanded perlite particles * * * interbonded one to another by interfusion between the surfaces of the perlite particles."[8] Neither Thomas nor Pierce disclose expanded perlite particles *interbonded one to another by interfusion between the surfaces thereof*; it is not therefore reasonable to view such interbonding to be obvious by considering the references collectively.

[2] Moreover, the "consisting essentially of * * *" terminology would, as the board pointed out, exclude additional unspecified ingredients which would affect the basic and novel characteristics of the product defined in the balance of the claim. However, to follow the teachings of Thomas combined in any manner with Pierce, would *require* the presence of at least one additional material with the expanded perlite, whether it be the sodium silicate binder of Thomas or the hydrated lime which Pierce uses to provide a chemical joining action. In either event it cannot be said that the additional ingredient would not materially affect the basic

[7] Saxe and Levitt, Product by Process Claims and Their Current Status in Chemical Patent Office Practice, 42 JPOS 528, 536, 537 (August 1960), and cases collected thereat.

See also a recent decision of this court in In re Steppan, 55 CCPA 791, 394 F.2d 1013, 156 USPQ 143 (1967), in which we found that use of the term "condensation product" in a chemical claim to a product did not thereby render the claim a product-by-process claim.

[1] [8] Taking the view we do that the just recited limitation is structural in nature we do not find it necessary to consider the additional recitation "while in a pyroplastic state * * *" as the mere presence of a method limitation in an article claim which is otherwise allowable would not so poison the claim as to render it unpatentable. Ex parte Lindberg, 157 USPQ 606 (P.O. Bd. App. 1967).

and novel characteristic of appellant's product which is that the perlite particles are held together *without* any additional material.

The rejections of claims 1 and 9 are therefore *reversed*. As to claims 2 and 5-8, the other claims initially appealed but not pursued, the appeal is dismissed.

MCLAUGHLIN, Judge, concurs in the result.

Court of Customs and Patent Appeals

In re JONES

No. 8099 Decided July 3, 1969

PATENTS

Particular patents—Polypropylene

Jones, Filled Polypropylene, claims 1 and 2 of application refused.—In re Jones (CCPA) 162 USPQ 224.

Appeal from Board of Appeals of the Patent Office.

Application for patent of Roger F. Jones, Serial No. 123,096, filed July 11, 1961; Patent Office Group 140. From decision rejecting claims 1 and 2, applicant appeals. Affirmed.

ROGER V. N. POWELSON and DONALD R. JOHNSON, both of Philadelphia, Pa., for appellant.

JOSEPH SCHIMMEL (JOSEPH F. NAKAMURA of counsel) for Commissioner of Patents.

Before WORLEY, Chief Judge, and RICH, ALMOND, and BALDWIN, Associate Judges.

BALDWIN, Judge.

Jones appeals from the Patent Office Board of Appeals decision affirming the examiner's rejection of claims 1 and 2, the only remaining claims in his application,[1] as unpatentable over Ward,[2] Blake,[3] and Orzechowski,[4] taken in combination, under 35 U.S.C. 103.[5]

The Invention

The invention relates to blends containing polypropylene and anthophyllite asbestos.[6] The specification indicates that articles molded from asbestos-filled polypropylene generally "exhibit enhanced tensile and flexural modulus"; however, under certain circumstances, specifically where the articles are to sustain prolonged exposure to moderately high heat,[7] the asbestos-filled compositions tend to oxidize and degrade more rapidly than unfilled polypropylene. Appellant has discovered that *anthophyllite* asbestos accelerates the oxidative degradation to a far lesser extent than do other asbestos.

The appealed claims read:

1. As a new composition of matter, a blend of crystalline polypropylene and anthophyllite asbestos, wherein the weight percent of asbestos is from 10% to 85%, together with a small but effective amount of an inhibitor against thermal and oxidative degradation.

2. The composition according to Claim 1 in which the weight percent asbestos is from 30% to 60%.

The References

Ward discloses compositions of asbestos with thermosetting resins, a number of which are listed as being applicable, and all types of asbestos are disclosed as acceptable. The preferred composition, however, comprises phenol-formaldehyde condensation resin with *anthophyllite* asbestos which has been chemically treated to eliminate acid soluble metallic constituents. The compositions

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[1] Serial No. 123,096, filed July 11, 1961, for "Filled Polypropylene."

[2] U. S. Patent 2,835,107, issued May 20, 1958.

[3] U. S. Patent 2,993,799, issued July 25, 1961, on an application filed August 20, 1957.

[4] U. S. patent 3,166,542, issued January 19, 1965, on an application filed February 3, 1961.

[5] In his brief, appellant has urged that "[i]n the latter part of its opinion the Board of Appeals is apparently rejecting the claims as not being supported by sufficient disclosure." We do not consider that the board was postulating a new ground of rejection under Rule 196(b) but rather was only commenting on the adequacy of the showing of unexpected results.

[6] Asbestos is the generic name given to a group of naturally-occurring, fibrous magnesium silicate minerals. There are two basic types: serpentine or long-fiber asbestos (chrysotile) and amphibole or short-fiber asbestos (tremolite, actinolite, amosite, crocidolite and anthopyllite). The latter type combine various amounts of iron, calium and sodium silicates with the magnesium silicate. They are said to be generally brittle and cannot be spun, as can chrysotile, but are more resistant to chemicals and heat. Condensed Chemical Dictionary 113 (6th ed. 1961).

[7] 280° and 310° F. are the only two temperatures mentioned in the specification. The intended use for the compositions may be "under the hood of an automobile in distributor caps, for example."

APPENDIX C RELATED PROCEEDINGS APPENDIX

There are no other pending appeals or interferences which will directly affect or be directly affected by or have a bearing on the Board's decision in this appeal, except for a prior Board decision, attached hereto, of June 30, 2004.

Appeal No. 2004-0032
Application No. 09/478,812

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Washington, DC 20036

Paper No. 28

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte YUKIYASU SUGANO, MASAHIRO FUJINO, MICHIO MANO, AKIHIKO ASANO, MASUMITSU INO, TAKENOBU URAZONO AND MAKOTO TAKATOKU

Appeal No. 2004-0032
Application No. 09/478,812[1]

HEARD: MAY 20, 2004

Before JERRY SMITH, BARRY, and SAADAT, Administrative Patent Judges.

SAADAT, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal from the Examiner's final rejection of claims 11, 12, 17, 18, 27, 28, 39, 40, 53, 54, 63, 65, 73 and 74. Claims 1-10, 13-16, 19-26, 29-38, 41-52, 55-62, 64 and 66-72 have been canceled.

We affirm.

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[1] Application for patent filed January 7, 2000, which claims the foreign filing priority benefit under 35 U.S.C. § 119 of the Japanese Applications No. P11-002384, filed January 8, 1999, No. P11-002385, filed January 8, 1999 and No. P11-02498, filed February 20, 1999.

BACKGROUND

Appellants' invention relates generally to a process for crystallizing semiconductor thin films in semiconductor devices, and more specifically, to a method of using laser irradiation for uniform crystallization of a prescribed region of the thin film.

Representative independent claim 11 is reproduced as follows:

> 11. A thin film semiconductor device comprising a semiconductor thin film, a gate insulating film accumulated on one surface thereof, and a gate electrode accumulated entirely within a prescribed region of said semiconductor thin film through said gate insulating thin film,
>
> wherein said semiconductor thin film is formed by forming a 30 to 80 nm layer of amorphous silicon or polycrystalline silicon having a first particle diameter on a substrate, and irradiating said substrate with an energy beam to convert said semiconductor thin film to polycrystalline silicon having a larger particle diameter than said first particle diameter,
>
> a thin film transistor is integrated and formed in said prescribed region by using said semiconductor thin film thus converted to polycrystalline silicon as an active layer, and
>
> a cross sectional shape of said energy beam is adjusted with respect to said region to irradiate said region in its entirety at a time by a single shot irradiation, so that characteristics of said thin film transistor are made uniform.

Appellants contrast the claimed single shot irradiation with the conventional process and assert that the structure resulting from the recited steps avoids the formation of borders in the crystallized silicon (brief, page 7). Appellants argue that the disclosure of Miyasaka is focused on irradiating unit areas individually with overlapping areas due to the movement of the substrate between each irradiation (brief, paragraph bridging pages 7 and 8).

The Examiner responds to Appellants' arguments by pointing out that the fact that the process steps define a particular structure does not mean that the final product is distinguished over the structure disclosed in the prior art (answer, page 8). The Examiner adds that Miyasaka, in fact, teaches a uniform, high-quality crystallized silicon film obtained by irradiating the substrate (id.). Additionally, the Examiner argues that the device made by the process of Miyasaka does not include borders since Miyasaka states that the laser irradiation provides for a "uniform" polycrystalline film (answer, page 9).

Appellants further argue that the uniform polycrystalline silicon substrate of the claimed invention is a result of irradiating the entirety of the unit size of the thin film and making a continuous film which avoids the formation of borders

in the crystallized silicon (reply brief, page 1). By referring to the instant specification, Appellants point out that such borders are the product of conventional crystallization process that involves the piecemeal irradiation of several adjacent regions of the unit size and slight overlapping of the regions that are separately irradiated (id.). Additionally, Appellants assert that the claimed process steps should be considered in evaluating the product claims to the extent that they attribute specific structural features to the final product (reply brief, page 2).

Before addressing the Examiner's rejections based upon prior art, it is an essential prerequisite that the claimed subject matter be fully understood. Analysis of whether a claim is patentable over the prior art under 35 U.S.C. §§ 102 and 103 begins with a determination of the scope of the claim. The properly interpreted claim must then be compared with the prior art. Claim interpretation must begin with the language of the claim itself. See Smithkline Diagnostics, Inc. v. Helena Laboratories Corp., 859 F.2d 878, 882, 8 USPQ2d 1468, 1472 (Fed. Cir. 1988). See also Pitney Bowes, Inc. v. Hewlett-Packard Co., 182 F.3d 1298, 1305, 51 USPQ2d 1161, 1165 (Fed. Cir. 1999) ("The starting point for any claim construction must be the claims

themselves."). Accordingly, we will initially direct our attention to Appellants' claim 11 to derive an understanding of the scope and content thereof.

Claim 11 is directed to a thin film semiconductor device comprising a thin film, a gate insulating film and a gate electrode "accumulated entirely within a prescribed region of said semiconductor thin film." Therefore, at least parts of a thin film transistor such as a gate electrode and the gate insulating layer are within the "region." The claim further requires that the region be irradiated "in its entirety at a time by a single shot" so that a thin film transistor with uniform characteristics may be obtained. Although the region that includes at least parts of a thin film transistor is required to be irradiated by a single shot, additional irradiation in preceding or subsequent steps are not precluded as long as each irradiation covers that region in its entirety.

A rejection for anticipation under section 102 requires that the four corners of a single prior art document describe every element of the claimed invention, either expressly or inherently, such that a person of ordinary skill in the art could practice the invention without undue experimentation. See Atlas Powder Co. v. Ireco Inc., 190 F.3d 1342, 1347, 51 USPQ2d

1943, 1947 (Fed. Cir. 1999); In re Paulsen, 30 F.3d 1475, 1478-79, 31 USPQ2d 1671, 1673 (Fed. Cir. 1994).

After reviewing Miyasaka, we agree with the Examiner that the reference teaches that a region of the silicon layer, which becomes the active layer of a thin film semiconductor device, is irradiated for crystallization of the thin film silicon (col. 36, lines 18-24). Miyasaka provides for irradiating an 8 mm x 8 mm portion of the silicon layer in a single shot irradiation before shifting the substrate over for irradiating an adjacent portion (col. 36, lines 29-34). As also conceded by Appellants (brief, page 7), Miyasaka further discloses that the entire substrate is irradiated by shifting the 8 mm x 8 mm square irradiation area in 4 mm increments in both the X and Y directions (col. 36, lines 42-45) in order to uniformly crystallize the silicon layer (col. 36, lines 45-48).

Therefore, Miyasaka teaches that a fairly large area (8 mm x 8 mm), which includes at least a gate electrode separated by a gate insulating layer from the thin film silicon layer, is irradiated by a single shot irradiation as the first exposure. Although this may constitute an intermediary product that is formed after the first exposure and before the substrate is shifted to step over the irradiation area during for the next

irradiation, such structure is not precluded by claim 11. In that regard, the claimed single shot irradiation reads on the very first area prior to shifting the substrate over for the next irradiation in an adjacent area.

Moreover, Miyasaka shifts the substrate in the horizontal direction until the entire length of the substrate in that direction is scanned and then in the vertical direction before the substrate is shifted in the horizontal direction again so that the entire surface of the substrate has been subjected to irradiation (col. 36, lines 32-38). Therefore, in addition to the intermediary product, i.e., the substrate after the first irradiation, a 4 mm x 4 mm part of the first area in the final product remains irradiated only once as the substrate is shifted by 4 mm both in the horizontal and the vertical direction away from this 4 mm x 4 mm part. Thus, contrary to Appellants' reasoning that it cannot be determined whether the structure of Miyasaka includes a single shot irradiation area at all (oral hearing), Miyasaka does disclose a thin film structure including at least a region in the substrate that is irradiated only by a single shot irradiation.

We are also unpersuaded by Appellants' argument that the claims require a single shot irradiation so that, as stated in page 51, lines 7-12 of the specification, the formation of borders in the crystallized silicon is avoided in the irradiated region (brief, page 7; oral hearing). Observing the Examiner's assertion that page 51 of the specification includes nothing related to avoiding borders and merely discusses uniformity of the crystallized silicon film (answer, page 9), we note that it is the claims that should be scrutinized to determine whether they require the exclusion of such border. Although page 51 of the specification does not mention avoiding borders, the problem of over-irradiating the boundary part is discussed in page 6 of the specification. It appears that Appellants, in an attempt to interpret the claims in light of the specification, actually do import limitations from the specification and define the claimed irradiation by "a single shot irradiation" as creating "boarder-less irradiated regions."

"We recognize that there is sometimes a fine line between reading a claim in light of the specification, and reading a limitation into the claim from the specification." Comark Communications, Inc. v. Harris Corp., 156 F.3d 1182, 1186, 48 USPQ2d 1001, 1005 (Fed. Cir. 1998). In locating this "fine

line" it is useful to remember that we look "to the specification to ascertain the meaning of the claim term as it is used by the inventor in the context of the entirety of his invention," and not merely to limit a claim term. Id. at 1187, 48 USPQ2d at 1005. Here in this case, the meaning of the claimed term is clear and extending it to encompass a boarder-less region places us on the other side of the line where reading this limitation into the claim from the specification would expand the claims beyond their scope.

Based on our findings related to Miyasaka and the analysis made above, we find that the Examiner has established a prima facie case of anticipation with respect to claim 11. Therefore, the 35 U.S.C. § 102 rejection of the representative claim 11 and claims 39, 53, 63 and 73, which fall together with claim 11, over Miyasaka is sustained.

With respect to the rejection of the remaining claims under 35 U.S.C. § 103, we note Appellants' designating of all the claims as falling with claim 11. Accordingly, we sustain the 35 U.S.C. § 103 rejection of claims 17 and 27 over Miyasaka and claims 12, 18, 28, 40, 54, 65 and 74 over Miyasaka and Tanaka.

CONCLUSION

In view of the foregoing, the decision of the Examiner rejecting claims 11, 39, 53, 63 and 73 under 35 U.S.C. § 102 and rejecting claims 12, 17, 18, 27 28, 40, 54, 65 and 74 under 35 U.S.C. § 103 is affirmed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a).

AFFIRMED

JERRY SMITH
Administrative Patent Judge)

LANCE LEONARD BARRY
Administrative Patent Judge) BOARD OF PATENT APPEALS AND INTERFERENCES

MAHSHID D. SAADAT
Administrative Patent Judge)

MDS/dpv

Appeal No. 2004-0032
Application No. 09/478,812

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